

CLAIMS

1. Process for testing an integrated circuit comprising memory points (140) and a Boundary Scan chain (120), in which one writes and/or reads to and/or from the memory points (140) by way of an access path (150) to the memory points (140) from an outside terminal (108) of the circuit, characterized in that the Boundary Scan chain (120) is activated so as to impose and/or observe logic levels on the inputs/outputs (120) of the integrated circuit.

2. Process according to claim 1, characterized in that the access path (150) to the memory points (140) and the Boundary Scan chain (120) are activated simultaneously.

3. Process according to claim 1 or 2, characterized in that the access path (150) to the memory points (140) and the Boundary Scan chain are activated by way of a line comprising in series the access path (150) to the memory points (140) and the Boundary Scan chain (120).

4. Process according to any one of claims 1 to 3, characterized in that the Boundary Scan chain (120) is activated by way of an activation path (150) linked to the Boundary Scan chain (120) downstream of a TAP controller (200).

5. Process according to claim 4, characterized in that the activation path (150) is linked to the Boundary Scan chain (120) at least by a logic gate (210, 220, 230, 240, 250) able to link, as a function of a control signal (ATPG-mode), the Boundary Scan chain (120) or else to the activation path (150) of the Boundary Scan, or else to the TAP controller (200).

6. Process according to either of claims 4 and 5, characterized in that the activation path (150)

includes at least one channel (ATPG-Si) on which is placed at least one memory point (140), this channel being able to be linked in series with the Boundary Scan chain (120) when the latter is activated.

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7. Process according to one of the preceding claims, characterized in that the input channel (Si), clock channel (ck) and configuration channel (Sh) of the Boundary Scan chain (120) are linked to logic gates (210, 220, 230, 240, 250) which are able to link, according to a control signal (ATPG-mode), these channels (Si, ck, Sh) or else to the input channel (Si), clock channel (ck) and configuration channel (Sh) of the TAP controller (200) or else to the input channel (Si), clock channel (ck) and configuration channel (Sh) of the activation path (150).

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8. Process according to one of the preceding claims, characterized in that all the memory points (140) are linked in series.

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9. Process according to one of the preceding claims, characterized in that at least some of the inputs/outputs (100) of the integrated circuit are connected directly to a tester able to inject chosen signals directly into certain of these inputs/outputs (100), and/or to receive output signals directly from certain of these inputs/outputs (100) and to compare these output signals with expected signals.

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10. Process according to one of the preceding claims in combination with claim 9, characterized in that the injection and/or direct measurement tester is coordinated with a device for controlling the Boundary Scan chain (120) so as to generate test vectors on sets comprising both inputs/outputs (103) connected directly to the tester and also inputs/outputs (105) connected to the tester via the Boundary Scan chain (120).

11. Process according to one of the preceding claims, characterized in that the circuit comprises accesses (150) to its set of memory points (140) and in that the test is carried out by controlling the set of memory points (140) so that the function of the integrated circuit is reduced to a combinatorial function.

12. Integrated circuit comprising a Boundary Scan chain (120) and an access path (150) to at least one memory point (140), characterized in that the access path (150) and the Boundary Scan chain (120) are linked in series and in that the circuit comprises means (220, 230, 240, 250) for intervening simultaneously on the memory point or points (140) of the access path (150) and on the cells (110) of the Boundary Scan chain (120).

13. Integrated circuit according to claim 12, characterized in that the means (220, 230, 240, 250) for intervening simultaneously on the memory point or points (140) of the access path (150) and on the cells (110) of the Boundary Scan chain (120) comprise at least one logic gate (220, 230, 240, 250) able to link the Boundary Scan chain (120) or else to the access path (150), or else to a TAP controller (200).

14. Integrated circuit according to claim 12 or 13, characterized in that the input channel (SI), clock channel (CK) and configuration channel (SHIFT) of the Boundary Scan chain (120) are linked to logic gates (220, 230, 240, 250) which are able to link, according to a control signal (MODE), these channels or else to the input channel (SI), clock channel (CK) and configuration channel (SHIFT) of the TAP controller (200), or else to the input channel (ATPG\_si), clock channel (ATPG\_ck) and configuration channel (ATPG\_se) of the access path (150).

15. Integrated circuit according to one of claims 12 to 14, characterized in that all the memory points (140) of the integrated circuit are linked in series.

5 16. Integrated circuit tester, comprising a first module for imposing and/or reading states of memory points (140) of an integrated circuit, characterized in that it comprises a second module for imposing states and/or reading states of input/output cells (110) by  
10 way of the Boundary Scan chain (120) of the circuit simultaneously with the action of the first module.

17. Integrated circuit tester according to claim 16, characterized in that it is contrived so as to  
15 simultaneously inject into an integrated circuit, control signals (SI) for the memory points (140) and control signals (SI) for the inputs/outputs (110) of the Boundary Scan (120).

20 18. Tester according to claim 17, characterized in that it is contrived so as to inject the control signals (51) for the memory points (140) and the control signals (51) for the inputs/outputs (110) of the Boundary Scan (120) onto one and the same channel.

25 19. Tester according to any one of claims 16 to 18, characterized in that it comprises a series of channels able to be connected directly to inputs/outputs (103) of an integrated circuit, and a module able to inject  
30 chosen signals directly into certain of these inputs/outputs (103), and/or to receive output signals from these inputs/outputs (103, 109) so as to compare these output signals with expected signals.

35 20. Tester according to claim 19, characterized in that it comprises a control device for the Boundary Scan chain (120) of an integrated circuit coordinated with the direct injection/reception module so as to generate test vectors on sets comprising both

inputs/outputs (103) connected directly to the tester and also inputs/outputs (105) connected to the tester via the Boundary Scan chain (120).

- 5 21. Tester according to one of claims 16 to 20, characterized in that it is able to control the set of memory points (140) in such a way that the function of the integrated circuit is reduced to a combinatorial function during the test.

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